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A 0.4v-6nw, Ultra-Low-Power, Bulk-Driven Current Recycling OTA

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Abstract: *This work presents the design of an ultra-low power Operational Transconductance Amplifier (OTA) in the weak inversion region, desirable for very low voltage applications specifically in the sub-threshold region of operation. The design targets of this work are set according to the circuit characteristics relevant to bio-signal processing, namely ECG, EEG, EMG or EOG signals. Some of the key design techniques include Bulk driven input stages, Current Recycling stages, Current Injection stages, Cascode loads, and a balanced left-to-right circuit symmetry. The simulation results confirm that the OTA achieves a gain of 57dB using only 0.4V voltage supply and a unity gain bandwidth of 3kHz, CMRR of 93dB(at DC), phase margin of 72^o, THD < 1% and finally consuming just 6nW of power. These results suggest that the OTA can be utilized as a building block in circuits meant to process bio-signals.*

Keywords: OTA, Weak inversion, Bulk Driven, Differential Current Recycling, Current Injection, Cascode Loads

1. Introduction

The need for low power portable electronic devices, more specifically biomedical devices is ever increasing. This serves as a huge motivator for researchers and circuit designers to pursue innovative work in ultra-low power front end circuits for these devices **[2,3,18]**. One such device which has consistently seen a tremendous amount of interest and thereby innovative designs is the operational trans-conductance amplifier (OTA). The OTA is the heart of instrumentation amplifiers used in bio-signal acquisition devices, where parameters like power consumption, noise performance, input dynamic range are critical **[2,3,4,18]**.

Table.1 lists some of the notable work done in bulk driven OTA designs the recent years. These figures obtained from these studies serves as a benchmark for our work done in OTA design in the weak inversion (WI) region of operation, specifically in the 180nm technology and employing the Bulk driven approach.

One of the hurdles of bio-signal processing arises from the low amplitude and low frequency characteristics of these signals. This creates a problem for designers to work with gate-driven devices. Therefore, our design employs bulk driven approach. Also, due to the lower transconductance of bulk driven devices compared to gate driven devices, various enhancement techniques have been used in this design approach. [3,4,5]

The work has been divided into 5 sections, Section 1 gives the introduction, Section-2 gives a brief description of the bulk driven MOS devices and an overview of the proposed OTA structure, the design techniques, power budget etc. along with the various stages that are involved to achieve the desired target of the OTA design. Section-3 includes circuit analysis and theoretical predictions for the expected gain, Section-4 highlights the simulation parameters used and discussion on the obtained results, Section-5 gives a brief discussion on the obtained results and also gives a comparison of the initial design targets and the achieved result.

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Table 1. Performance Comparison of a few notable Bulk Driven OTA designs.

Paper Title	Supply (Volt)	Gain (dB)	PM	BW (kHz)	CMRR (dB)	Power (nW)	THD (%)
An Ultra-Low-Voltage Transconductance Stable and Enhanced OTA for ECG Signal Processing [13]	0.4	54.7	>45°	14.4	58	20.23	--
31.3 nW, 0.5 V Bulk-Driven OTA for Bio-signal Processing [6]	0.5	54.7	>50°	6.18	75	31.3	0.2
A 0.5-V Multiple-Input Bulk-Driven OTA in 0.18-μmCMOS [16]	0.5	40	>60°	1	--	24.77	0.219
A 0.5-V 95-dB rail-to-rail DDA for bio signal processing [17]	0.5	45	>60°	12.66	--	--	--

2. Proposed OTA

At the core of the OTA circuit is the bulk driven input stage: Here the bulk input signal modulates the threshold voltage which in turn modulates the Drain current I_D. The expressions relating the threshold voltage, the bulk source voltage and the Drain current are given by equation (1) and (2): **[18,19]**

$$V_{TH} = V_{TH0} + \gamma(\sqrt{\{2\phi_F + V_{SB}\}} - \sqrt{\{2\,\phi_F\}} \quad (1)$$

V_{SB} = Source to Bulk voltage
γ = Body Effect Coefficient
ϕ_F = Fermi Potential

$$I_D = \left(\frac{1}{2}\right)\mu c_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad \text{(strong inversion)} \quad (2)$$

$$I_D = 2n\mu C_{ox}\, V_T^2\left(\frac{W}{L}\right)e^{\frac{V_{GS}-V_{TH}}{nV_T}}(1 - e^{-\frac{V_{DS}}{V_T}}) \quad \text{(weak inversion)} \quad (3)$$

μ = carrier mobility
c_{ox} = oxide capacitance per unit area
$\frac{W}{L}$ = transistor aspect ratio
V_{GS} = Gate to Source voltage
λ = channel length modulation parameter
n = substrate factor
V_T = thermal voltage

The advantage of modulating the drain current via the bulk terminal is that it eliminates the need for gate overdrive voltage and enables operation at voltages lower than the threshold voltage.

The proposed OTA is shown in figure 1. it can be viewed as two identical halves, split in the middle by the input signal. At zero differential voltage, both halves behave exactly the same. [2,3,4,5,6] Once the differential signal is introduced, the operation on one half is complementary to the other half. Each half has five main stages:

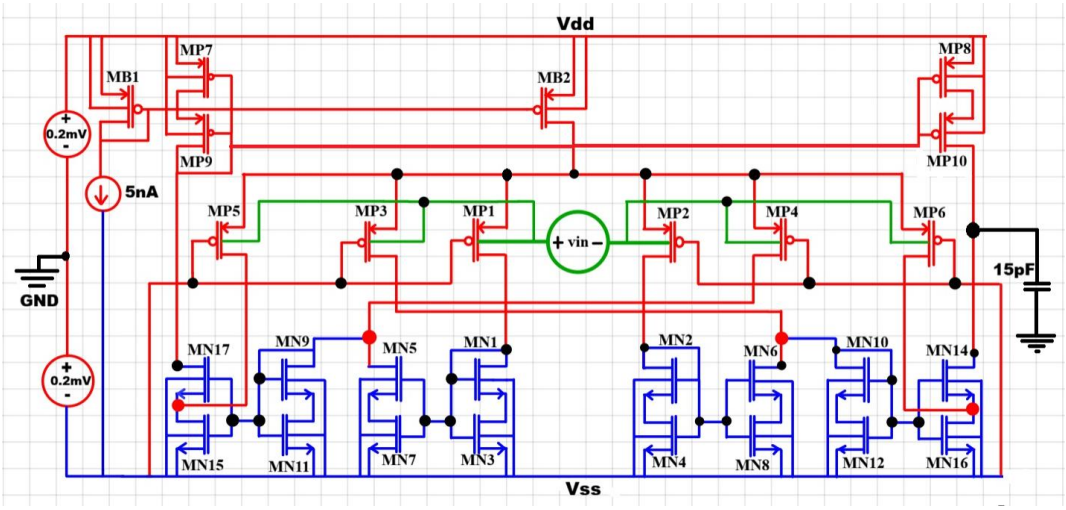

Figure 1. Circuit Diagram of the Proposed OTA

2.1 First stage: Power supply and Biasing: Supply voltage V_{DD} = 0.2V and V_{SS} = −0.2V, which results in a total supply voltage of 400mV. The circuit is biased by a 5nA current source through M_{B1} which is then mirrored (mirror ratio 1:3) by MB2 to generate a core current of 15nA. At zero input this core current splits evenly into two halves of the input.

2.2 Second stage: Input stage: [4,5,6] The input stage is a current scaling network, consisting of M_{P1}, M_{P3}, M_{P5} on one half of the input stage and M_{P2}, M_{P4}, M_{P6} lies on the other half. Both sides have the following W/L ratios as M_{P1}:M_{P3}:M_{P5}::1:2:2 & M_{P2}:M_{P4}:M_{P6}::1:2:2. Therefore, at zero differential input, we have 7.5nA (half of 15nA) further divided between three transistors depending on the W/L ratios. i.e. M_{P1}:M_{P3}:M_{P5}::1.5nA:3nA:3nA. Similarly, for the other half, M_{P2}:M_{P4}:M_{P6}::1.5nA:3nA:3nA (this constitutes the quiescent current I_0). When a differential signal is introduced at the bulk terminal of M_{P1}, M_{P3} and M_{P5} and M_{P2}, M_{P4}, M_{P6} i.e. v_{in}+ and v_{in}−, the current I_0 through the devices change as follows:

$$I_{MP1} = I_0 + \Delta I,\ I_{MP3} = I_0 + 2\Delta I,\ I_{MP5} = I_0 + 2\Delta I$$
$$I_{MP2} = I_0 - \Delta I,\ I_{MP4} = I_0 - 2\Delta I,\ I_{MP6} = I_0 - 2\Delta I$$

where ΔI denote the incremental change in the drain current in response to the change in the input differential input voltage. The size of ΔI depend on the bulk trans-conductance $g_{mbs1,2}$, which lower than the transconductance gm of the device, hence we apply transconductance enhancement techniques to drive up the g_{mb}.

2.3 Third stage: [6,7,8,9,10,11,12] Current Recycling Network: This stage of the circuit is responsible for the current re-use/re-cycle mechanism. This stage is responsible for enhancing the transconductance of the OTA design. It includes the Cascode structures M_{N1}-M_{N3} and M_{N5}-M_{N7} on one side, M_{N2}-M_{N4} and M_{N6}-M_{N8} on the other. The current through

M_{N1}/M_{N2} is from M_{P1}/M_{P2} while the scaled current from M_{P4}/M_{P3} is fed to M_{N5}/M_{N6}. The scaled current from M_{P4}/M_{P3} is designed to be double the current from M_{P1}/M_{P2} as $(W/L)_{MP1}$:$(W/L)_{MP4}$::1:2. Because of the increase in size of $M_{P4,5}/M_{P3,6}$ compared to $M_{P1,2}$, the mirrored currents are also proportionately increased. This ensures that the drain terminal of M_{N1}/M_{N2} and the drain terminal of M_{N5}/M_{N6} are not receiving the same input signal. So even before the differential signal is introduced, the node voltages differ from one another. The gate voltage however, of $M_{N1,3}/M_{N2,4}$ and $M_{N5,7}/M_{N6,8}$ is fixed by the current sourced by M_{P1}/M_{P2}. This is possible because although the gate terminals are tied together the W/L ratios differ so the current through the devices also differ. When the differential signal comes into these nodes ($Drain_{MN1}$ and $Drain_{MN5}$) through M_{P1} and M_{P4}, the difference in the node voltages widen as one node receives $+\Delta I$ and the other receives $-2\Delta I$ or vice versa. So for the same input signal we achieve greater voltage swing at these nodes by reusing/recycling the input signal current. The OTA also has two current scaling mirror networks $M_{N1,3}/M_{N5,7}$ and $M_{N9,11}/MN_{17,15}$ on one side, $M_{N2,4}/M_{N6,8}$ and $M_{N10,12}/M_{N14,16}$ on the other side with mirror ratios 1:1.5 and 1:5. The combined current reuse technique and current mirror scaling technique enhances the effective transconductance as shown by equation (3)**[6-12]**,

$$g_{m(effective)} = \beta_{m1}\beta_{m2}\beta_1 g_{mb,MP1} \quad (3)$$

here β_{m1} = mirror scaling factor of $M_{N1,3}$ and $M_{N5,7}$ ($M_{N2,4}$ and $M_{N6,8}$)
β_{m2} = mirror scaling factor of $M_{N9,11}$and $M_{N17,15}$ ($M_{N10,12}$ and $M_{N14,16}$)
β_1 = current reuse factor $(W/L)_{MP4}$:$(W/L)_{MP1}$

2.4 Fourth stage: Current Summation Node: [11,12] The node connecting drain of M_{P5}/M_{P6}, Drain of M_{N15}/M_{N16} and the source of M_{N17}/M_{N14} can be seen as the node responsible for injecting the recycled current into the output stage branches. Here M_{P5}/M_{P6} injects the mirrored current into the node, M_{N15}/M_{N16} isolates that current and M_{N17}/M_{N14} converts that signal current variation into voltage variation. The current injected by M_{P5}/M_{P6} adds with the current through M_{N17}/M_{N14} and M_{N15}/M_{N16} sinks the total current. Due to this, the node voltage ($M_{P5Drain}$-$M_{N15Drain}$-$M_{N17Ssource}$)/ ($M_{P6Drain}$-$M_{N16Drain}$-$M_{N14Ssource}$) drops/increases to accommodate this additional current through M_{N15}. This drop/increase allows V_{GS} of $M_{N17,15}/M_{N14,16}$ to increase/decrease and thereby increase/decrease the current in the output path which increases the output node voltage swing. Therefore, the mirrored current from M_{P5} can modulate the output voltage. So, when the differential signal comes into the input PMOS devices, the output node voltage is strongly modulated even by a small variation in the mirrored current because of the careful design of the aspect ratios at every stage. The contribution to the overall transconductance due to the action of this fourth stage is given by equation (4):

$$G_{m,total} = \beta_{m1}\beta_{m2}\beta_1 g_{mb1,MP1}(1 + k\,\beta_2) \quad (4)$$

k = the fraction of the signal current generated by $\beta_{m1}\beta_{m2}\beta_1 g_{mb,MP1}$ steered through M_{P5} and is expressed as: $k \approx \frac{\beta_3}{\beta_1\beta_{m1}\beta_{m2}}$, where β_3 = current reuse factor $(W/L)_{MP5}$:$(W/L)_{MP1}$

β_2 = fraction of the steered M_{P5} current that adds to the output current.
The term $k\beta_2$ tells us what fraction of the current I_{eff} (current due to combined action of current mirror and current reuse network) actually flows from M_{P5} to the Source-Drain of M_{N17}-M_{N15}, and also how much of that current is actually flowing through M_{N17} (the output node). So the final expression for the total transconductance by the three stages can be

expressed by equation (5)

$$G_{m,total} = \beta_{m1}\beta_{m2}\beta_1 g_{mb1,MP1}(1 + k\,\beta_2) \quad (5)$$

In summary, the input stage creates a current with g_{mb}, the current reuse stage multiplies the same current and the current injection stage scales that current to the output node. The effect of β_2 is not uniform for the low impedance output node and the high impedance node. since we have used an active load design, whereby a larger current swing on the low impedance node ensures a larger voltage swing on the high impedance node. For this very reason we have used the low impedance node for our β_2 calculation in the circuit analysis. The effect of increase or decrease in the signal current across the low impedance node is amplified by the active load structure.

2.5 Fifth stage: **Cascode Boosted Impedance Stage[10,15,16,19]**: This is the final stage of the circuit where we have used Cascode NMOS stack namely $M_{N17,15}/M_{N14,16}$ and PMOS cascodes $M_{N14,16}/M_{P8,10}$ on the other side to boost the output impedance of the circuit. The output is taken from the high impedance output node ie. Drain of M_{N14} and drain of M_{P10}. The high output impedance ensures that even a small change in the differential current will produce a huge output voltage change thereby ensuring that the overall gain remains high. The effective out impedance is given by equation (6):

$$R_{out\text{-}total} = R_{out,pmos} \parallel R_{out,nmos}$$
$$R_{out,nmos} \approx \mathbf{r_o}_{MN16}.\mathbf{r_o}_{MN14}.\mathbf{g_m}_{MN16}$$
$$R_{out,pmos} \approx \mathbf{r_o}_{MP10}.\mathbf{r_o}_{MP8}.\mathbf{g_m}_{MP10}$$

So the over gain of the OTA can be expressed as:

$$Gain_{overall}(A_v) = G_{m,total} \text{ x } R_{out\text{-}total}$$
$$A_v = \beta_{m1}\beta_{m2}\beta_1 g_{mb1,MP1}(1 + k\,\beta_2)(\mathbf{r_o}_{MP10}.\mathbf{r_o}_{MP8}.\mathbf{g_m}_{MP10} \parallel \mathbf{r_o}_{MN16}.\mathbf{r_o}_{MN14}.\mathbf{g_m}_{MN16}) \quad (6)$$

3. Circuit Analysis

3.1 Power supply:
V_{DD} = +0.2V, V_{SS} = -0.2V, Supply voltage (total) = 0.4V

3.2 Bulk Tranconductance:
Bulk coupling factor (η) ≈ 0.303, $g_{mb1} = \eta g_{m1}$ = 10.67nS

3.3 DC Bias Current:
W/L_{MB1}:W/L_{MB2} = 5:1 :: 15:1, I_{bias}:I_{core} = 5nA:15nA,
At, v_{id} = 0V, I_{core} = 15nA, $I_{lefthalf}$ (M_{P1},M_{P3},M_{P5}) = 7.5nA, $I_{righthalf}$(M_{P2},M_{P4},M_{P6}) = 7.5nA,
W/L_{MP1}::W/L_{MP3}::W/L_{MP5} = 6:1::12:1::12:1, I_{MP1}:1_{MP3}:I_{MP5} = 6:12:12 = 1:2:2,
I_{MP1}:1_{MP3}:I_{MP5} ≈ 1.5nA:3nA:3nA.

3.4 Recycling Factor (β_1):
$\beta_1 = W/L_{MP4}$:W/L_{MP1} = 12:1::6:1 = 2:1 = 2,
$g_{m(effective)} = \beta_{m1}\beta_{m2}\beta_1 g_{mb1,MP1} = 1.5 \times 5 \times 2\, g_{mb1}$
$g_{m(effective)}$ = 15 × 10.67 nS = 160.05 nS

3.5 Current Summation Factor ($1+k\beta_2$):

$\mathbf{k} \approx \frac{\beta_3}{\beta_1\beta_{m1}\beta_{m2}}$ = 0.133 (M_{P4} and M_{P5} have the same W/L ratios, so $\beta_3 = \beta_2$)

$\boldsymbol{\beta_2}$ = (calculated at the low impedance node, i.e. $Drain_{MN17}$ and $Drain_{MP9}$) signifies the fraction of the M_{P5} current entering M_{N17}, which is decided by the impedance offered by M_{N15} as opposed to the impedance offered by the M_{N17} in series with the M_{P9} and M_{P7}.

$$\beta_2 \approx \frac{r_{oMN15}}{\frac{1}{g_{mMN17}}+\frac{1}{g_{mMP9}}+\frac{1}{g_{mMP7}}} \qquad (7)$$

$\beta_2 \approx 4.55$ i.e.$(1+k\beta_2) = 1.606$

3.6 Out-put Impedance:

$R_{out\text{-}total} \approx (\mathbf{r_{o}}_{MP10}.\mathbf{r_{o}}_{MP8}.\mathbf{g_{m}}_{MP10} \parallel r_{o}{}_{MN16}.r_{o}{}_{MN14}.\mathbf{g_{m}}_{MN16})$,

$R_{out\text{-}total} = 2.45\ G\Omega \parallel 43.32\ G\Omega = 2.32\ G\Omega$

3.7 Overall Gain

$A_v = \beta_{m1}\beta_{m2}\beta_1 g_{mb1,MP1}(1 + k\,\beta_2)$ $(\mathbf{r_{o}}_{MP10}.\mathbf{r_{o}}_{MP8}.\mathbf{g_{m}}_{MP10} \parallel r_{o}{}_{MN16}.r_{o}{}_{MN14}.\mathbf{g_{m}}_{MN16})$,

A_v = 160.05 nS x 1.6 x 2.32 GΩ = 594 = **55.5dB**

3.8 Power Consumption:

$P_{dc} = I_{bias}$ x Supply voltage (total), P_{dc} = 15nA x 0.4 V = **6 NanoWatt**.

4. Simulation Parameters and Results

The proposed OTA was simulated in Tanner EDA tool using 180 nm CMOS process technology. Table.2 shows the simulation parameters used in the OTA design simulation. The following analysis were carried out: Frequency response, DC transfer characteristics, Common Mode Rejection response, Input Referred Noise Response, Slew Rate Response and Total Harmonic Distortion Response. The results are displayed in figure 2, figure 3, figure 4, figure 5, figure 6 and figure 7.

Table 2. Simulation Parameters

Si.No.	Parameters	Values
1.	Bias current I_B	20nA
2.	V_{DD},V_{SS}	0.2V,-0.2V
3.	Load Capacitance	15pF
4.	W/L ratios for M_{B1}, M_{B2}	5:1, 15:1
5.	W/L ratio for M_{P1},M_{P2}	6:1
6.	W/L ratio for M_{P3},M_{P4},M_{P5},M_{P6}	12:1
7.	W/L ratios for M_{P9},M_{P10}	320:1
8.	W/L ratios for M_{P7},M_{P8}	16:1
9.	W/L ratios for M_{N1},M_{N2}	40:1
10.	W/L ratios for M_{N3},M_{N4}	2:1
11.	W/L ratios for M_{N5},M_{N6}	60:1
12.	W/L ratios for M_{N7},M_{N8}	3:1

13.	W/L ratios for M_{N9},M_{N10}	20:1
14.	W/L ratios for M_{N11},M_{N12}	1:1
15.	W/L ratios for M_{N17},M_{N14}	100:1
16.	W/L ratios for M_{N15},M_{N16}	5:1

4.1: Frequency Response (gain and phase): Figure 2, shows the intrinsic gain of the circuit at 57 dB with Unity Gain Bandwidth at 3kHz. The OTA also demonstrates a phase margin of 72^o ensuring a stable operation. This supports our reason for employing the current reuse technique and the enhanced output impedance techniques

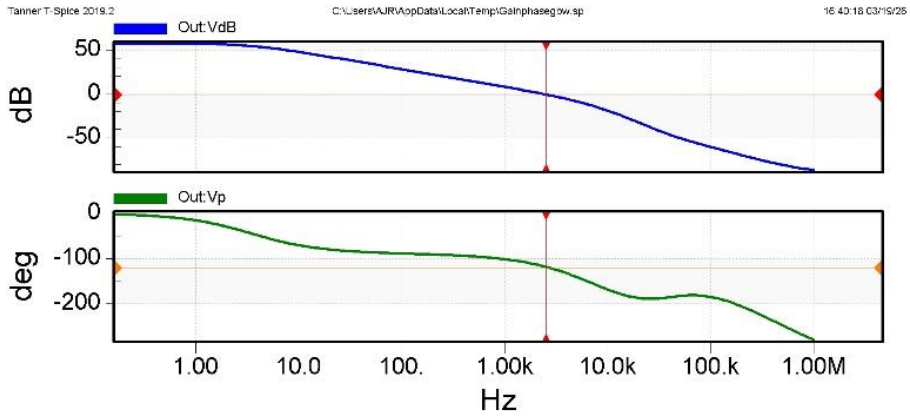

Figure 2: Frequency response (gain and phase) of the OTA

4.2 DC Transfer Characteristics: Figure 3, shows that the proposed OTA demonstrates a highly linear response over an input range of ±150mV. This indicates good matching between the input and output response.

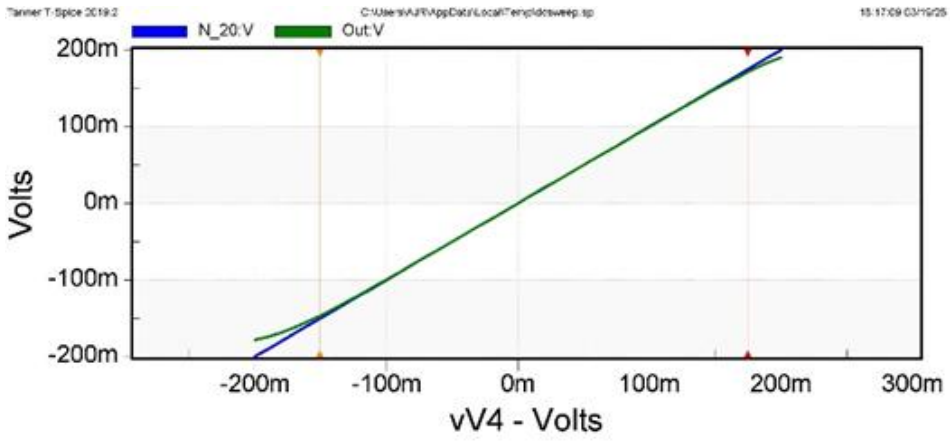

Figure 3: DC Transfer Characteristics of the OTA

4.3 Common Mode Rejection Ratio (CMRR) Response: Figure 4 shows a CMRR of 92dB at DC and 40dB at 1kHz is maintained, which is adequate for low frequency biomedical signal acquisition where signal bandwidth can be in range of a few 100 Hz.

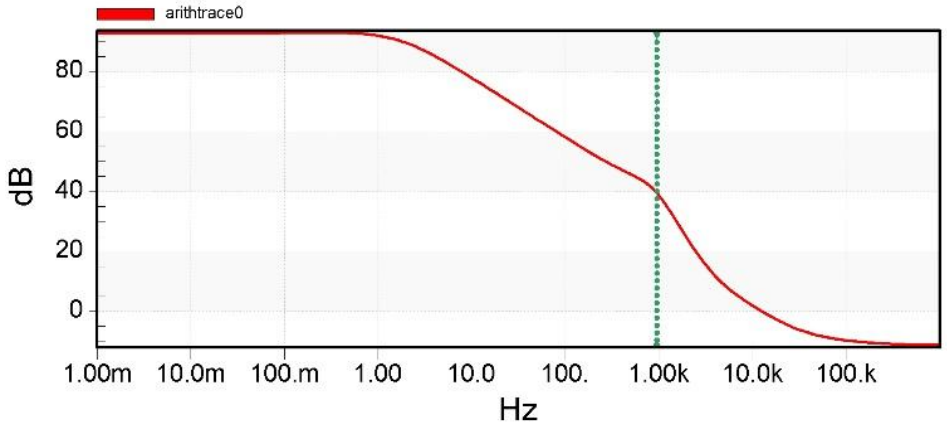

Figure 4: CMRR response of the OTA

4.4 Input Referred Noise: Figure 5, shows the input-referred noise spectral density at 2.2µV/√Hz up to 1kHz, which indicates effective suppression of flicker noise.

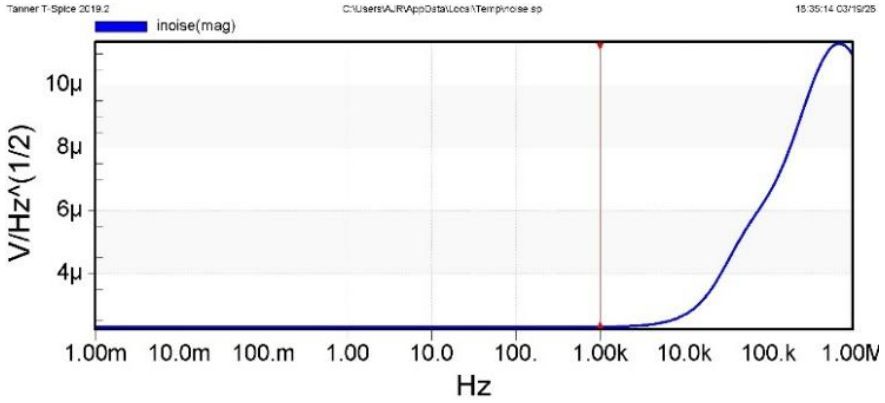

Figure 5: Noise response of the OTA

4.5 Slew Rate Response: Figure 6, shows the slew rate response of 0.075mV/µs, which exceeds the minimum requirement for biomedical signal processing which usually range from 0.001mV/µs to 0.1mV/µs.

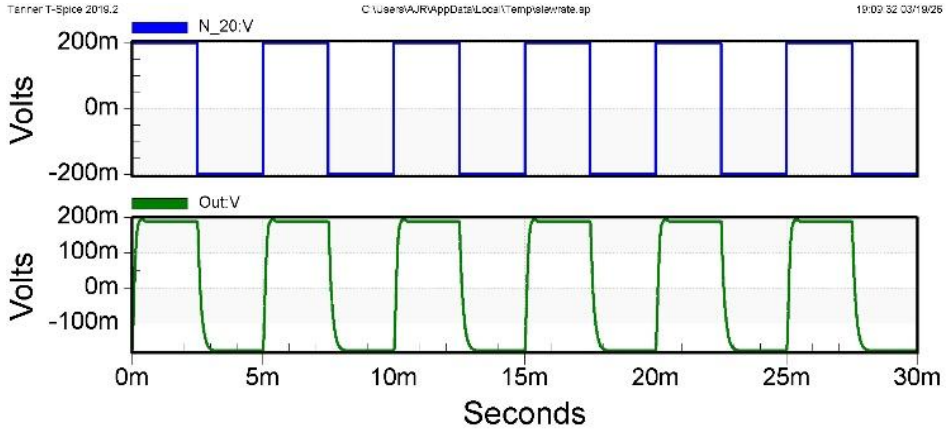

Figure 6: Slew Rate response of the OTA

4.6 Total Harmonic Distortion (THD): Figure 7 gives the THD response of the OTA. The simulation shows that the THD response is 0.77% which is suitable for biomedical signals

where THD <1% is considered acceptable.

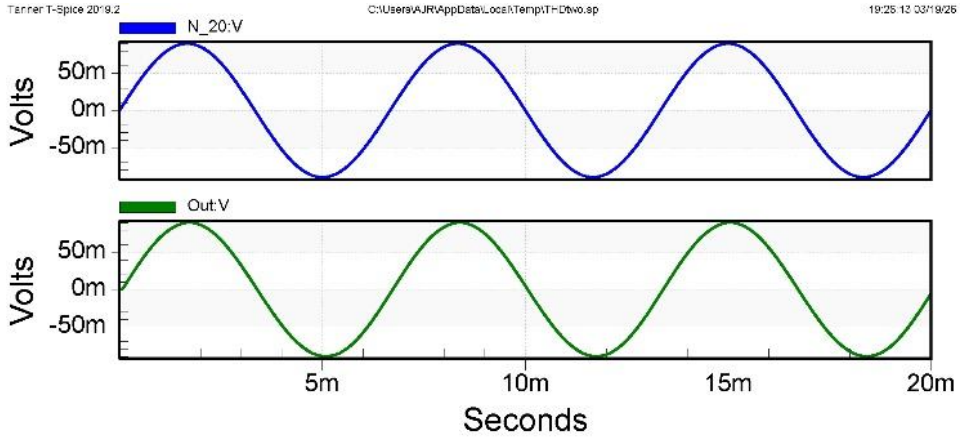

Figure 7: THD response of the OTA

4.7: Simulation Results Summary: Table 3 summarizes the results obtained from our circuit simulation and compares with the intended design targets of a low power OTA used in bio signal processing circuits.

Table 3: Simulation Results

Si. No.	parameter	Goal	Achieved
1.	Gain	40-60dB (for use in standalone OTA	57dB @0.4V power Supply
2.	Power consumption	< 2µ	6nW
3.	GBW	1 kHz (to safely cover up to 300 Hz)	3 kHz
4.	CMRR	> 60 dB	93 dB at DC 40dB @ 1KHz
5.	Subthreshold operation	(0.4V – 0.6V)VDD	0.4V VDD
6.	Phase margin	$> 60^{o}$	72^{o}
7.	Noise tolerance	70-100nV/√Hz	75nV/√Hz
8.	THD	<1%	0.77%

5. Conclusion

The circuit analysis and the simulation results confirm that OTA achieves a voltage gain of about 57dB, a GBW of 3khz and power consumption of 6nW, which suggests that the proposed design has all the characteristics required for designing instrumentation amplifiers, filters used in biosignal processing. If the bias current is increased at the cost of the DC power, the circuit can be designed for better noise margins and higher GBW. Care has to be taken while deciding the W/L ratios for such changes as the circuit parameters has been meticulously selected to ensure the maximum efficiency and best possible trade-offs.

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